Improving Multilevel Writes on Vertical 3-D Cross-Point Resistive Memory

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***Abstract*—Resistive memory is promising to be constructed as a high-density storage-class memory. Multilevel cell, access-transistor-free cross-point array structure, and 3-D array integration are three approaches to scale up the density of resistive memory. However, composing the three approaches together strengthens the interactions between array-level and cell-level nonidealities (interconnect resistance-induced IR drop, sneak current, and device variability) of resistive memory arrays during write operations and significantly degrades write performance and reliability. In this article, we analyze the dynamic voltage-dividing effect along a selected write current path in 3-D cross-point memory arrays. We propose a nonideality-tolerant high-density resistive memory (HD-RRAM) architecture, that can weaken the interactions between nonidealities and mitigate their degradation effects on the performance and reliability of array multilevel write operations. HD-RRAM is equipped with a double-transistor array architecture with two-transistor-*n*-resistor (2TnR) cell organization along pillars to reduce the current driving requirement and the large undesired voltage drop across each vertical pillar access transistor. Moreover, multi-side asymmetric bias improves the resistive switching velocity by leveraging current-dividing effects. Variability-aware multilevel state partition reduces the worst-case write error rate by leveraging target state dependency of variability. Proportional-control multilevel state tuning reduces the average number of required write-and-verify iterations by leveraging pulse amplitude dependency of variability. Multilevel cell parallel writing improves the cell-level parallelism by leveraging the pass-through feature of intermediate resistance states. The evaluations show that HD-RRAM reduces both memory access latency and energy consumption over an aggressive baseline.**

***Index Terms*—Crossbar, high-density memory devices, memory array operation scheme, nonideal device characteristics, performance optimization, voltage drop analysis.**

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I. Introduction

In THE big-data era, the ever-growing data-intensive applications raise higher requirements for the capacity of memory systems. Resistive memory is promising to break through the memory scalability bottleneck faced by one-transistor–one-capacitor (1T1C) DRAM [1], [2]. Metal-oxide resistive random-access memory (RRAM) has small cell area, 3-D integration potential, long data-retention time ($\geq$ 1 year), and low read latency ($\leq$ 20 ns) [2]. Therefore, resistive memory can be built as high-density storage-class memory to reduce the slow I/O data movement when a page fault occurs.

As bit-line parasitic capacitance and memory capacitor charge leakage are two important device nonidealities of 1T1C DRAM arrays for read operations, IR drop, sneak current, and device variability are three important nonidealities of high-density resistive memory arrays for write operations [2], [3]. These array-level and cell-level nonidealities of resistive memory arrays become worse when the feature size scales down and significantly degrade the performance and reliability of write operations [3]–[5]. Interconnect resistance-induced IR drop lowers the effective write voltage and causes its cell-to-cell nonuniformity, which significantly enlarges the write latency [2], [6]–[10]. Moreover, IR drop and sneak current depend on interconnect geometry [2], [11], which shows a tradeoff between density and write reliability. Device variability becomes significant in nanoscale [12]. RRAM variability depends on the resistance state [13], [14], which may enlarge the write error during multilevel write operations.

To scale up the density of resistive memory, there are three common approaches: 1) multilevel memory cell (MLC); 2) access-transistor-free cross-point memory array structure; and 3) 3-D memory array integration. However, the interactions between array-level and cell-level nonideal effects during write operations are more complex when the three high-density approaches are composed together. First, the sneak currents through half-selected cells enlarge the IR drop along the selected plane or lines, while the IR drop along the selected plane or lines decays the sneak currents through half-selected cells [2]. If conventional single-side bias (SSB) scheme is applied on cross-point memory arrays, the effective write voltage is highly nonuniform among cells in the array and depends on multiple dynamic write operation parameters [2]. Moreover, the write latency setting of multilevel cell cross-point memory arrays is more sensitive to the IR drop-induced

cell-to-cell nonuniformity of effective write voltage than that of single-level cell cross-point arrays. Second, multilevel write latencies of multilevel cells are more sensitive to the switching variability than those of single-level cells. Device variability makes the IR drop fluctuate, exacerbates the tail write latency problem and causes write error, while IR drop complicates the pulse amplitude-dependent switching variability. Third, 3-D cross-point memory arrays have more sneak current branches than the 2-D cross-point array with the same layer size and thus have larger IR drop [2]. Therefore, the interactions between coupled nonidealities of memory cells and interconnects in the memory arrays and their impact on write performance need to be better quantification and understood, in order to provide guidelines for the design of memory array operation scheme.

In this article, we implement multilevel memory based on 3-D cross-point memory arrays, since multilevel memory is achieved by applying voltage pulses on the memory array to tune the cell resistance into the target state [15]. We choose the vertical 3-D cross-point array architecture because of its lower cost-per-bit than the horizontal counterpart [12]. We first build a dynamic memory array model and analyze the interactions between cells and interconnects and the dynamic voltage-dividing effect in multilevel cell 3-D cross-point memory arrays during write operations. We observe that in the conventional single-transistor array (SITA) architecture, the small-size vertical pillar access transistor (VPAT) divides up a large portion of array bias voltage during write operations, causing switching speed degradation. Also, the cell-to-cell nonuniformity of effective write voltage in 3-D cross-point arrays is significantly larger and is more complex than that in 2-D cross-point arrays with the same layer size. Since the switching speed is an exponential function of the cell effective voltage [16], the cell-to-cell nonuniformity of effective write voltage makes it difficult to share a group of multilevel write latencies among all the multilevel cells in an array [2]. In this scenario, the high-performance cells near to voltage drivers will suffer from significant write performance loss if the memory controller only adopts the multilevel write latencies of the lowest performance cell in the arrays. Therefore, we carry out static parameter and dynamic operation co-optimization from the viewpoint of the interactions between nonidealities of devices and interconnects in memory arrays, to improve the performance and reliability of multilevel write operations on ultrahigh-density resistive memory while keeping its natural advantage of energy efficiency [2]. The contributions of this article are summarized as follows.

1) We propose a double-transistor array (DOTA) architecture with two-transistor-*n*-resistor (2TnR) cell organization along pillar electrodes for 3-D cross-point memory, to reduce the current driving requirement and the large undesired voltage drop across the small-size VPATs without extra area cost. We further propose multiside asymmetric bias (MAB) to improve the resistive switching velocity of the selected cells by leveraging the current-dividing effects.
2) We provide variability-aware multilevel state partition (VASP) based on logarithmic cell resistance metric to reduce the write error rate by exploiting the target-state dependency of switching variability. We design proportional-control multilevel state tuning (POST) to reduce the average number of required write-and-verify iterations in a voltage pulse ramp by leveraging the pulse-amplitude dependency of switching variability.
3) We devise multilevel cell parallel writing (MPW) in cross-point memory arrays by leveraging the pass-through feature of intermediate resistance states.
4) We evaluate the proposed high-density resistive memory architecture with comprehensive performance metrics both at the array level and the full-system level.

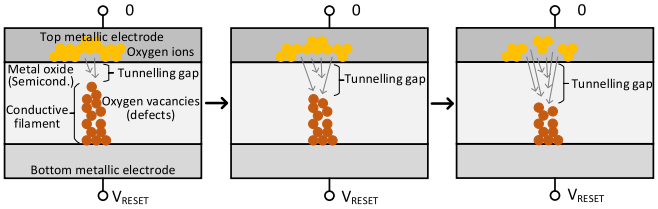

Fig. 1. Multilevel RESET process of a resistive memory cell achieved by tuning the voltage pulse duration.

II. High-Density Memory Approaches

Multilevel resistive memory cells use multilevel resistance states to store information, as shown in Fig. 1. The electron tunneling gap length can be taken as an internal physical state variable to represent the stored data pattern, and the cell resistance is an exponential function of the gap length [16]. The continuously tunable dynamic range is subdivided into four states to store two bits in a cell. The switching to decrease cell resistance is called SET, whereas the switching to increase cell resistance is called RESET. The write latency is much longer than the read latency [16]. For the switching dynamics, the write velocity is an exponential function of the applied voltage amplitude across the cell [16]. Therefore, *the effective write voltage across the selected cell* is a key metric for analyzing multilevel write operations and characterizing multilevel write latencies of the selected cell.

Access-transistor-free cross-point memory arrays are constructed by two groups of interconnects (word-lines and bit-lines) perpendicular to each other with memory cells sandwiched in between [18], [19]. The removal of access transistors can reduce the equivalent cell area to $4/n\ F^2$, where n is the number of memory layers, and F is the feature size. Interconnects include 1-D interconnect lines and 2-D interconnect planes. For the same material, the latter has lower unit resistance than the former. 1/2 voltage bias scheme can be used to write the target cells in a cross-point memory array. The selected word-line and selected bit-lines are biased at 0 and V, respectively, while unselected lines are biased at $V/2$ [2]. For read operations, we adopt the unselected word-line grounding with unselected bit-line floating (WG-BF) read scheme that outperforms with large read margin and low array power consumption among conventional read bias schemes [20]. Usually, a small group of neighboring cells on the selected word-line in a cross-point memory array is written at a time [6], due to the word-line IR drop

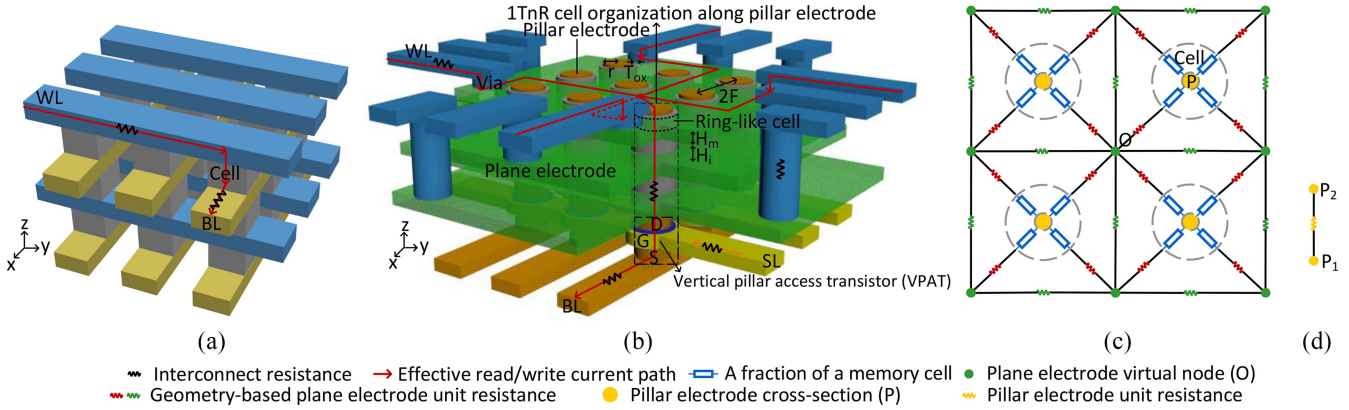

Fig. 2. 3-D cross-point memory arrays. (a) Horizontal line-type. (b) Vertical plane-type [17]. (c) Resistor network model for the multiholed plane core and ring-like cells, where OP is described as a subcircuit. (d) Interplane connection. WL: word-line, BL: bit-line, SL: select-line.

criterion and the limited current drivability of the peripheral CMOS word-line driver [21], [22]. The read latency of the selected multilevel cell in a cross-point memory array is independent to the cell effective read voltage, and it is calculated by the interconnect *RC* delay plus the peripheral transimpedance amplifier delay [21].

3-D cross-point memory arrays can be classified into the wafer-like horizontal type [2], [23] and the multiholed vertical type [12], [17], [24]–[26]. The array architectures are shown in Fig. 2(a) and (b), respectively. The vertical type has lower cost-per-bit than the horizontal counterpart [12]. Also, the vertical type uses the perforated plane electrodes as 2-D interconnects, which reduces the unit interconnect resistance and thus the IR drop [12], [27], [28]. Thus, we mainly focus on the vertical type in this article. In the vertical type, ring-like cells are sandwiched between mutually perpendicular plane electrodes and pillar electrodes. A VPAT is serially connected with n parallel-connected memory cells to form a one-transistor-n-resistor (1TnR) structure along a pillar, and a select-line selects a vertical 2-D cross-point array.

III. Analysis of Multilevel Write Operations on 3-D Cross-Point Memory Arrays

To better understand the detailed dynamic interactions between MLCs, interconnects, and access transistors during multilevel write operations and better evaluate new techniques, we build a dynamic memory array model that can simulate write operations and analyze write process in multilevel cell 3-D cross-point memory arrays. Nonlinear *I–V* characteristics and nonlinear switching dynamics of the bipolar-switching memory cell are described by the generic Verilog-A device model [16]. The C2C variability is introduced into the memory cell Verilog-A module [16] by incorporating the variability as a random fluctuation into the mean gap length change in the cell ($\mathrm{d}g/\mathrm{d}t$) [16] that expresses the resistance state change in a time step, where the random variable is realized by generating the random number following the Gaussian distribution with the given deviation [29]–[32]. BSIM4 nMOS transistor model [16], in the predictive technology model [33], is incorporated into the array netlist for HSPICE simulation. The bias voltage that the transistor can endure is up to 5 V. We use the same interconnect materials as the previous work [14], [25], [34]. The interconnect resistance and coupling capacitance are calculated based on geometry. The cell-level and array-level parameters in the model are shown in Table I. The feature size of memory cell is calculated as $F = r + T_{ox} + G_P$, and $2F$ is typically larger than the vertical transistor width (W) [24].

TABLE I
Parameters in the 3-D Cross-Point Dynamic Memory Array Model

Parameter description	Range (Typical value)
Memory cell properties	HfO_2-based [16]
Gap length in the memory cell (l_{gap})	0.6∼1.23 nm
Variation factor of the memory cell (σ_f)	0∼5×10^4 (2.5×10^4) Ω/V
TiN pillar electrode top radius (r)	9∼33 (25) nm
Pillar etching slope (AR)	1280
HfO_2-based cell thickness (T_{ox})	5 nm
Inter-pillar half-gap at the top layer (G_P)	7∼31 (15) nm
Pt Plane electrode thickness (H_m)	5∼65 (20) nm
Insulation layer thickness (H_i)	5∼65 (14) nm
Cu word-line or bit-line thickness (H_l)	65 nm
Width of vertical NMOS transistors (W)	64 nm
Length of vertical NMOS transistors (L)	32 nm
Number of select-lines (n_s)	4∼128 (32)
Number of plane electrodes (n_l)	4∼64 (16)
Number of bit-lines (n_b)	4∼128 (32)
Maximum number of selected multilevel cells in an array during write op. (n_{max})	4
Inter-plane unit coupling capacitance (C_c)	0.3 fF
Array write bias voltage (V_{RESET})	2.55 V
Select-line voltage during RESET (V_{gRESET})	3.55 V
Unselected select-line voltage	0 V
Array read bias voltage (V_{read})	0.2 V
Select-line voltage during read (V_{gread})	1 V

The ring-like memory cells in vertical 3-D cross-point arrays are different from the cuboid memory cells in the horizontal type, and the multiholed continuous 2-D interconnect planes are also different from the 1-D interconnect lines in the horizontal type. To generate the array netlist for HSPICE analysis, the ring-like cells and plane electrodes should be discretized. The resistor network model for multiholed interconnect planes and ring-like cells is shown in Fig. 2(c). Every ring-like cell is discretized into four fractions along the current flow directions. The four fractions of a cell can be approximately viewed as parallel connected, thus the resistance of each fraction is 4

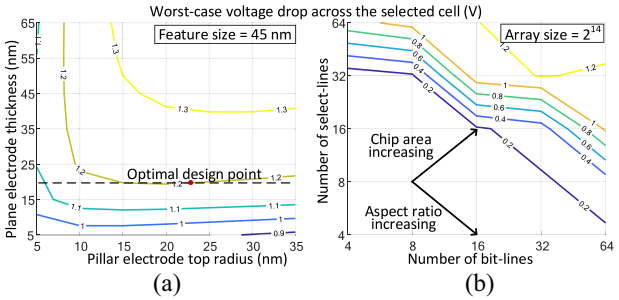

Fig. 3. Effective voltage as a function of geometric parameters: (a) plane thickness and pillar radius and (b) array aspect ratio and chip area.

times of the whole cell resistance. The plane margin has the same mesh structure as the plane core. Interplane unit coupling capacitance is connected at the center point (O) of four neighboring pillar electrodes and between two neighboring plane electrodes.

However, the HSPICE system solving with operation simulation time and memory usage of simulating the dynamic array model of vertical 3-D cross-point memory arrays are more than one-order-of-magnitude larger than those of simulating the static array model of horizontal-type 3-D arrays or 2-D arrays with the same number of memory cells. First, the grid discretization of plane electrodes and ring-like cells significantly increases the number of nodes in the network which is equal to the number of KCL equations (i.e., system scale) and also the number of branches (include behavioral cell fractions). Second, the network topology of vertical 3-D cross-point arrays is denser than that of horizontal-type 3-D arrays or 2-D arrays. The node degree of post-discretized vertical 3-D cross-point arrays is up to 8, whereas the node degree of horizontal-type 3-D arrays and 2-D arrays is no larger than 4 and 3, respectively. The node degree plus 1 equals to the number of nonzero entries on the row corresponding to that node in the system coefficient matrix (i.e., reflect sparsity). Third, as the dynamic Verilog-A memory device array and two transistor arrays are incorporated into the array netlist, they significantly increase the computational complexity. To reduce the simulation time and memory space usage of operating 3-D cross-point memory arrays with plane electrodes and ring-like cells, we suggest that bias-operation-adaptive current-density-aware resistor network construction with only the principal components of the array may reduce the number of nodes and the degree of nodes in the network.

There are two array geometry tradeoffs between the mutually perpendicular plane electrodes and pillar electrodes for reducing the IR drop: 1) pillar radius and 2) plane thickness [3]. If the pillar electrode radius is too small, the pillar resistance is high. However, with the same feature size, if the pillar electrode radius is too large, the interpillar half-gap is small, thus the plane electrode resistance is high. Besides, if the plane electrode is too thin, the plane resistance is high. However, if the plane electrode is too thick, the pillar electrode is tall, thus the pillar electrode resistance is high. Therefore, we sweep the geometric parameters to identify the optimal design point with the highest effective voltage. The results are plotted in Fig. 3. In Fig. 3(a), we can see that the effective voltage is sensitive to pillar radius and plane thickness. Fig. 3(b) indicates that for the same array size, the effective voltage is higher when the plane size is larger, since the plane resistivity is lower than the pillar resistivity. As the cost-per-bit increases with the plane thickness increasing, we choose the array aspect ratio (length:width:height) as 2:2:1, and the selected design point is shown in Table I.

Since the switching velocity is an exponential function of the effective write voltage across the selected cell [16], we analyze the voltage drop breakdown along the write current path in the conventional SITA architecture with SSB scheme. We observe the following.

1) In the SITA architecture, the small-size VPAT divides up more than 30% of the array bias voltage, and only a small portion of voltage falls on the selected cell during write operations.
2) The effective voltage and the corresponding multilevel write latencies are highly nonuniform with the SSB scheme (i.e., single-point voltage delivery), due to the interaction between interconnect IR drop and cell sneak currents in the memory arrays. The cell-to-cell latency nonuniformity ($>10\times$) makes it hard to share multilevel write latencies among cells in an array.
3) In the 3-D cross-point memory arrays, the effective write voltage across the selected cell significantly increases with time during a RESET process, due to the time-varying resistive switching process of the selected cells and the dynamic voltage-dividing effect among the VPAT, the interconnects (plane and line), and the memory cell along the selected write current path. Thus, the multilevel write latencies of multilevel cell cross-point memory arrays are quite different from the multilevel write latencies of a standalone multilevel cell.

IV. HD-RRAM Architecture

By weakening the interactions between IR drop and the other two nonidealities and conquering multiple nonideality issues in each part of our design, respectively, we can cope with each nonideality of resistive memory. After the interactions between nonidealities are weakened, the design complexity of the nonideality-tolerant memory array operation scheme is reduced by dividing the design of multilevel write scheme into four independent design stages to form a complete set of solutions: ❶ array voltage bias (DOTA-based MAB); ❷ multilevel cell state partition (VASP); ❸ multilevel cell state tuning (POST); and ❹ MPW. The bank-level architecture of high-density RRAM (HD-RRAM) design is illustrated in Fig. 4. Motivated by 1) the current-dividing effect along the vertical pillars, 2) the pulse-amplitude-dependent feature of switching variability, and 3) the pass-through feature of intermediate resistance states, HD-RRAM improves the performance of write operations on multilevel cell 3-D cross-point memory arrays from three dimensions: 1) improving the resistive-switching velocity under an array write pulse; 2) reducing the average number of write-and-verify iterations in a voltage pulse ramp; and 3) improving the cell-level

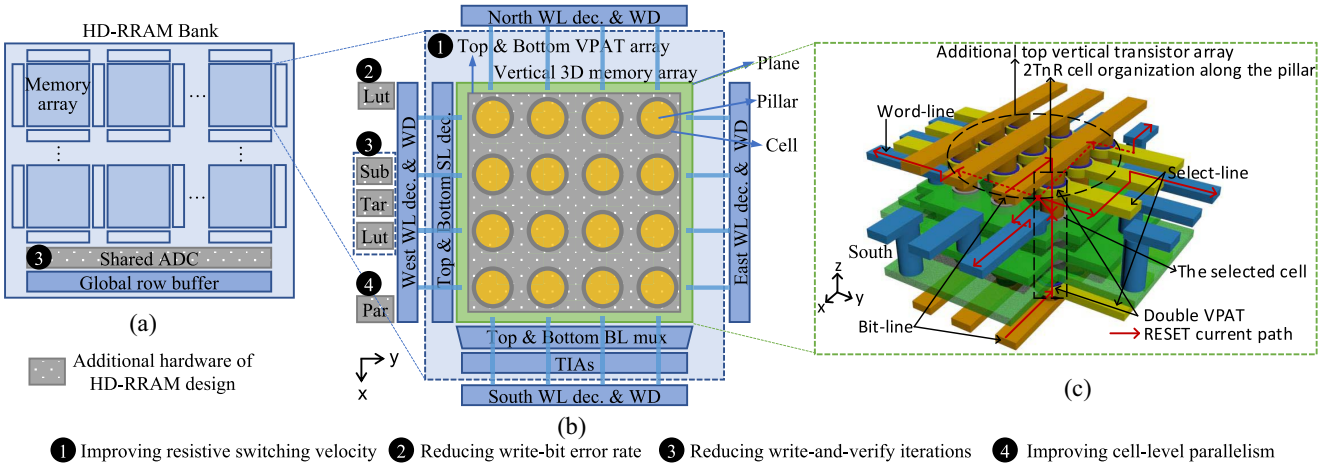

Fig. 4. HD-RRAM architectural overview. (a) Array organization in a memory bank. (b) Memory array and periphery. (c) DOTA architecture with distributed voltage delivery on the selected pillars and the selected plane. WL: word-line, BL: bit-line, SL: select-line, VPAT: vertical pillar access transistor, TIA: transimpedance amplifier, WD: write driver, dec.: decoder, Sub: subtractor, Tar: target register, Lut: Lookup table, Par: parallelizing logic.

write parallelism, respectively. The performance improvement of multilevel write operations can be decomposed into the product of the three dimensions.

A. Double-Transistor Array Architecture

The write operating current of metal–oxide resistive memory devices typically ranges from 10 to 100 μA, and it does not significantly decrease with the downscaling of device cross-sectional area due to the filamentary conduction mechanism [12]. Three-dimensional vertical cross-point arrays utilize a VPAT array underneath the memory array to provide 2-D address decoding and drive sufficient write current. Since the VPATs have to be aligned to the pillar electrodes to retain high memory density, the channel width of the VPAT is horizontally limited by the array feature size, which limits the current drivability of the VPATs. Although the driving current of the VPAT can be increased by tuning the select-line and boosting its gate-source voltage by up to 5 V, it is still limited yet [24], [35]. The small-size VPAT (i.e., pillar current driver) has to drive all the $n_l - 1$ sneak currents through $n_l - 1$ half-selected cells and only one effective write current through a selected cell along the selected pillar electrode during 1/2 write bias operations, where n_l is the number of memory layers. We observe that the VPAT divides up more than 30% of the array bias voltage in the conventional SITA architecture with one-transistor-n-resistor (1TnR) cell organization along pillar electrodes where currents are only driven from the bottom end of the selected pillars [Fig. 2(b)] [17], [36]. The write current driving requirement of the selected pillars further increases as n_l increasing, since there are more sneak current branches connected to and thus more sneak currents flowing out of the selected pillar electrodes. We further observe that the enhancement which only connects four sides of the selected plane electrode to the voltage source simultaneously (multi-directional write driver (MWD) scheme [17]) further enlarges the undesired voltage drop that the VPAT divides up at the same array bias voltage. This is because in this case, the four parts of the selected plane electrode can be viewed as parallel connected, and the plane equivalent resistance and word-line equivalent resistance are reduced. Therefore, the VPAT has to drive larger current. The large voltage drop across the VPAT lowers the effective write voltage across the selected cell due to the voltage-dividing effect along the selected write current path, ultimately enlarging the write latency and array write power consumption.

To reduce the current driving requirement of the small-size VPATs, we propose the DOTA architecture for 3-D cross-point memory arrays, as shown in Fig. 4(c). The sandwiched array structure is successively composed of the bottom-layer VPAT array, the intermediate 3-D memory array, and the top-layer VPAT array. The main enhancement is placing another VPAT array on top of the vertical 3-D cross-point memory array to work with the bottom-layer VPAT array and form a 2TnR cell organization along a pillar electrode, where n is the number of memory layers (n_l). Two parallel VPATs are serially connected with n parallel-connected memory cells to divide and drive all the $n_l - 1$ sneak currents and the effective write current along a selected pillar electrode from both the top and the bottom ends of the pillar simultaneously, leveraging the current-dividing effect along the selected pillar electrodes. As the top-layer and bottom-layer VPATs can be viewed as parallel connected, the equivalent channel width of VPAT connected to a pillar is equivalently doubled. Thus, the equivalent drain–source resistance of VPAT is reduced, and the current drivability of VPAT is improved. As the additional top-layer VPAT array is aligned to the top end of the pillar electrode array, the top-layer VPAT array only increases the height of the whole array and does not incur extra area cost.

The top-layer VPAT array is typically fabricated separately from the 3-D memory array with pillar electrode array [34] and tacked onto the pillar electrode array [37]. Since vertical 3-D cross-point resistive memory is compatible with the back-end-of-line, we can put the standalone-fabricated VPAT array on the memory array without incurring fabrication issues [37], [38]. The top-layer VPAT arrays and their decoders

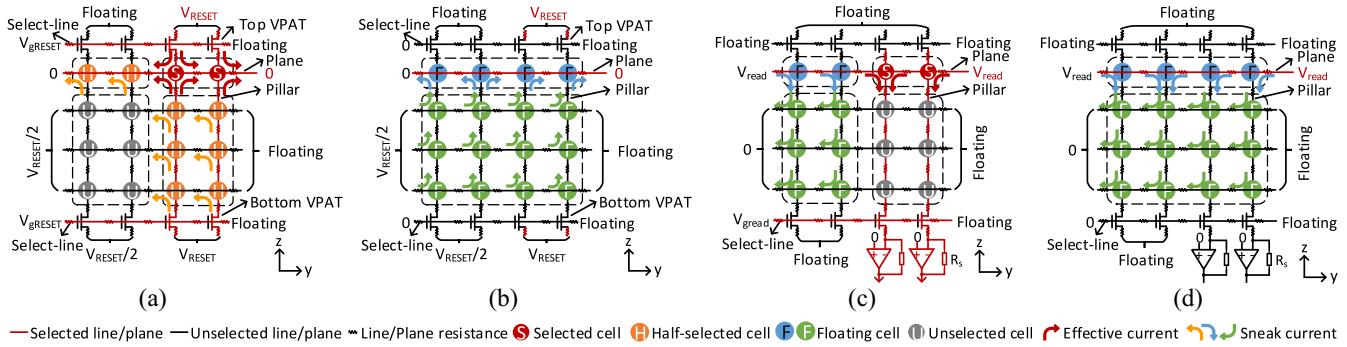

Fig. 5. MAB scheme. (a) and (b) For 1/2 bias *write operations* on the selected vertical slice and unselected slices, respectively. (c) and (d) For WG-BF *read operations* on the selected vertical slice and unselected slices, respectively. The two (bottom and top) groups of bit-lines connected to the two VPAT arrays are along the x-axis and not shown here.

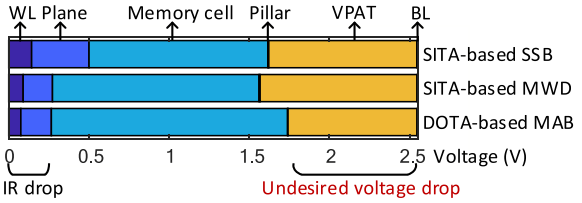

Fig. 6. Voltage-dividing effects on a *write* current path at the beginning of RESET operations for the conventional SSB [25], MWD [17], and MAB under their worst-case cell location, respectively. VPAT refers to each VPAT.

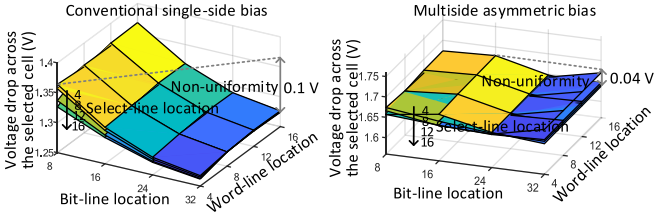

Fig. 7. Cell-to-cell nonuniformity of effective write voltage under (a) SSB and (b) MAB, due to the interaction between interconnect IR drop and cell sneak currents in the 3-D cross-point array.

incur 16.9% extra cost-per-bit [24]. In our configuration, the feature size is determined by the bottom-most memory layer. Considering the limited pillar etching aspect ratio, as the top-layer VPAT array is aligned and tacked onto the pillar electrode array, the channel width of the top-layer VPATs is slightly larger than that of the bottom-layer VPATs. This scenario slightly enlarges the current drivability of the top-layer VPATs and improves the effect of the MAB scheme. Also, the non-ideal etching effect may partially compensate the lower current drivability of the top-layer VPATs caused by possible larger leakage current of top-layer VPATs.

B. Multiside Asymmetric Bias

To reduce the undesired voltage drop along the selected multidirectional write current paths in multilevel cell 3-D cross-point memory arrays, we propose an MAB scheme. The side view of the MAB scheme for the vertical-sliced 2-D cross-point components of the vertical 3-D cross-point array is shown in Fig. 5. The MAB scheme is essentially a line connection scheme [3]. For write operations, the MAB scheme connects two ends of the selected pillar electrodes and four sides of the selected plane electrode to the voltage sources simultaneously. Meanwhile, MAB only connects one end of unselected pillar electrodes and one side of unselected plane electrodes to the voltage source. For 1/2 bias method, full write bias voltage is applied to the selected electrodes while half write bias voltage is applied to unselected electrodes. The bias voltage of the top-layer select-line is set as the same as that of the bottom-layer select-line. The distributed voltage delivery of MAB makes the two terminals of a selected memory cell have multidirectional effective current write paths, thanks to the current-dividing effects along the selected pillars and the selected plane. For DOTA-based MAB, the effective write voltage across the selected cell is 1.47 V, 1.33 V, and 1.17 V at the beginning of RESET operations when the number of memory layers (n_l) is 16, 32, and 64 with 32×32 layer size, respectively. To guarantee the cell effective voltage is larger than the RESET threshold voltage, up to 64 RRAM cells along a pillar can be controlled by the 2 VPATs, i.e., 2T-64R structures. The limiting factor of n_l is the increasing driving requirement of n_l-1 sneak currents through n_l-1 half-selected cells connected to a selected pillar electrode. 1/2-based MAB write scheme can be similarly extended to 1/3-based MAB write scheme.

For read operations, MAB scheme only connects one end of a pillar to the TIA for virtual grounding, and the top-layer VPAT array is not used, as shown in Fig. 5(c). This is because for WG-BF read method, other than a selected cell, there are only unselected cells and thus no sneak current along a selected pillar. The readout current of a selected bit-line is equal to a single effective read current, thus the IR drop along a selected pillar can be neglected [21] during WG-BF read operations. WG-BF MAB read scheme does not require additional TIAs, compared with conventional single-side read bias schemes [20]. However, there are floating cells on the selected plane and sneak currents along the selected plane, thus the IR drop along the selected plane is still large, especially when multiple cells on the plane are selected to read at a time. Therefore, MAB read scheme still connects four sides of the selected plane to the voltage source.

Owing to the current-dividing effects and the distributed voltage delivery, DOTA-based MAB can reduce the write latency using even lower array bias voltage. Compared with SITA-based MWD [17], DOTA-based MAB can improve the worst-case effective write voltage from 1.28 to 1.47 V when the array bias voltage is 2.55 V, as shown in Fig. 6. MAB can also lower the array bias voltage from 3 to 2.55 V with similar write performance. Besides, MAB reduces the worst-case cell-to-cell nonuniformity of effective write voltage in the array by 60%, as shown in Fig. 7. MAB makes the effective write voltage almost independent to the selected cell location by weakening the interactions between IR drop and the other two nonidealities, thus all the multilevel cells in the array can share the same group of multilevel write latencies. The comparisons of performance and energy consumption between SITA-based MWD [17] and DOTA-based MAB are demonstrated in Fig. 8. The figure reveals the dynamic voltage-dividing effect along the selected write current path in the memory array during write operations. DOTA-based MAB improves the transient RESET velocity by around 6.3 times. The instantaneous array power consumption during a dynamic write process includes the power consumption of all components in the memory array, and the results are shown in Fig. 8(d). The overall array power consumption has only a small decline during the RESET process, since the total current decreases while the effective write voltage increases. For DOTA-based MAB, the current-dividing effect along the selected pillar electrodes reduces the power consumption of the VPATs. Consequently, the total RESET power is reduced by 30.8%. The array energy consumption during a dynamic write process is reduced by 6.9 times, which is calculated as the time integral of the instantaneous array power consumption.

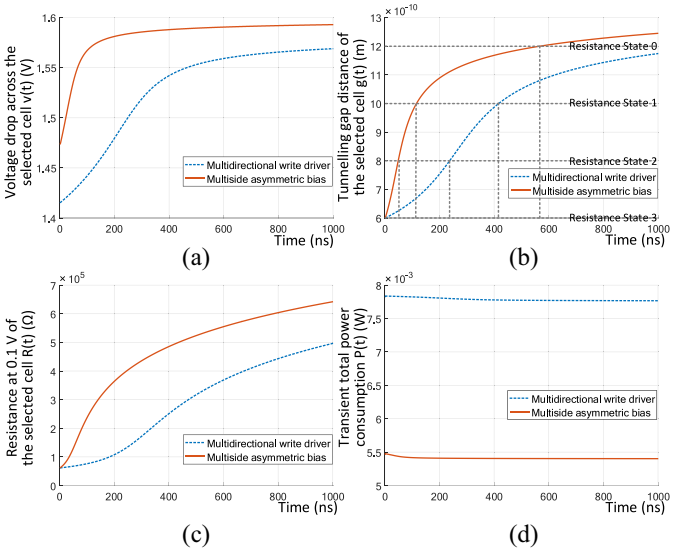

Fig. 8. Array-level time-domain dynamic write process of the worst-case location cell with all other cells in the lowest resistance state. Time evolution of (a) effective write voltage, (b) tunneling gap length, (c) cell resistance, and (d) transient array total power consumption with MWD and MAB schemes. Array bias voltage for MWD and MAB is 2.9 V and 2.55 V, respectively.

C. Variability-Aware Multilevel State Partition

The variability of resistive memory cells has two dimensions: 1) extrinsic spatial device-to-device (D2D) variability and 2) intrinsic temporal cycle-to-cycle (C2C) variability [4], [5]. Metal–oxide resistive memory suffers from much larger C2C switching variability than D2D variability due to its filament conduction mechanism [4], and the large variability significantly degrades write reliability. Generally, there are two influence factors of C2C variability: 1) the target resistance state and 2) the applied pulse amplitude [14]. C2C variability determines the maximum number of state levels that the dynamic range can be subdivided into, since two adjacent states are indistinguishable if they are overlapped with each other. C2C variability of a resistive memory cell makes the target state resistance after a write operation follow lognormal distribution [39]–[41]. Moreover, C2C variability is nonuniform across different states (i.e., interstate nonuniformity in a cell), and the variability exhibits some statistical rules. C2C variability increases with resistance state increasing [13], [39], [42], [43]. This is because when the memory device works in HRS, the conductive filament is thin, thus a small migration of the oxygen vacancies from the filament may significantly change the tunneling gap length and thus cell resistance [14]. The relative variation (σ/μ) can be approximated as a linear function of the mean value of the logarithm of cell resistance $\log_{10}(R_{\text{cell}})$: $\sigma/\mu = k\mu + b$, where σ and μ are the standard deviation and the mean value of the logarithm of cell resistance, respectively, and $k = 1.9\times10^{-3}$ and $b = 1\times10^{-4}$ are constants [14], [44]. Here, σ is the deviation under the condition of a single long write pulse to switch one state to the adjacent state.

Since the cell resistance is an exponential function of the tunneling gap length in the cell [16], the conventional uniform multilevel state partition scheme [15] using the logarithmic metric of cell resistance $\log_{10}(R_{\text{cell}})$ (resulting in linear increment of tunneling gap length) to equally divide the dynamic range into multilevel resistance states does not fully consider the state-to-state nonuniformity of C2C variability. If using conventional tunneling gap-equidistant state partition, the state margin in high-resistance regime is narrower than that in low-resistance regime, and two adjacent resistance state bands may even overlap with each other, as shown in Fig. 9(a). Also, in high-resistance regime, when a voltage pulse is applied on the cell in a multilevel write process, the cell resistance may overshoot the target state due to C2C variability and may easily fall into the next state, causing write error. In this scenario, a new voltage pulse is needed to tune the cell resistance back to within the target state and thus to recover the write error [39]. However, the extra recovering-write operation incurs extra energy and latency cost [45].

To reduce the write error rate by reducing the state overshoot probability in a multilevel write process, we design VASP scheme based on the $\log_{10}(R_{\text{cell}})$ cell state metric, shown in Fig. 9(b). The scheme makes high-resistance states wider whereas low-resistance states narrower by fixing the two boundary resistance states and appropriately moving the position of intermediate states to low resistance regime. To determine the mean position of intermediate states, we further formulate the state quantization rule as: $\mu_i - \mu_{i-1} =$

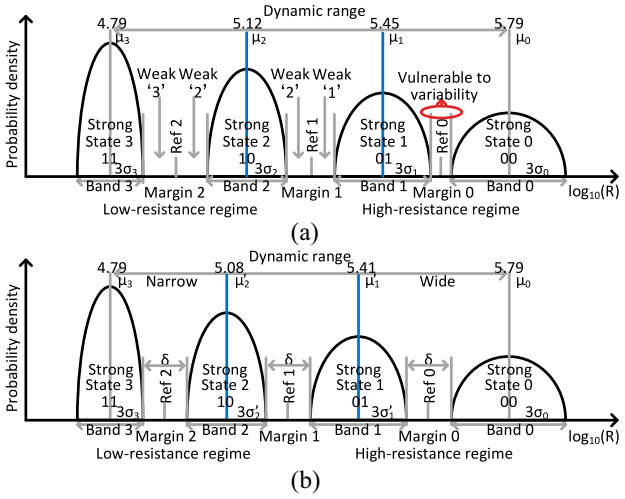

Fig. 9. (a) Conventional ESP [15], [39] and (b) variability-aware state partition with equal state margin based on the logarithm of cell resistance for resistive memory. Proper read margins between neighboring states can be further used to tolerate noises during read operations [21].

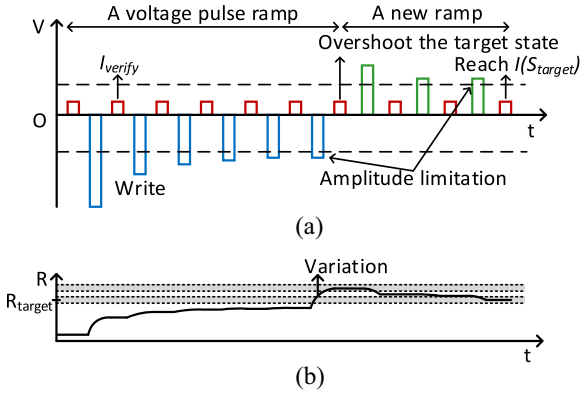

Fig. 10. (a) Proportional-control multilevel state tuning. (b) Illustration of cell resistance evolution.

$3\sigma_{i-1} + \delta + 3\sigma_i$, where μ and σ are the mean value and the standard deviation of the lognormal resistance distribution of a state, respectively, and the constant δ is the common state margin between adjacent physical states to tolerate the variability. As the positions of the two boundary states are known, μ_i for every intermediate states and the state margin δ can be determined by solving the system of quadratic equations. VASP makes every resistance states have the same tolerance to variability. Since VASP does not produce new resistance state levels, it does not affect the total number of intermediate resistance states. For the multilevel cell vertical 3-D cross-point arrays, we use Monte Carlo simulation [8] for emulating the stochastic write process in our model. We generate the time-domain trace file including the evolution of the effective write voltage and cell resistance of each time step (1 ns) in HSPICE transient analysis mode for each dynamic multilevel write operation process. We take each trace file corresponding to a stochastic write process as a sample. We run 500 times of the transient analysis process to get the resistance statistics. The result shows that VASP design can reduce the write error rate from around 2.6×10^{-3} to 8×10^{-4} compared with conventional gap-length equal-difference partition scheme.

D. Proportional-Control Multilevel State Tuning

Iterative write-and-verify resistance-state tuning methods are commonly used to overcome C2C variability during multilevel write operations that switches the current state to the target state [39], [45]. C2C variability has a feature that the absolute variation of the resistance change is proportional to the applied pulse amplitude: $\sigma = \sigma_f V_d$, where σ_f is the variation factor, and V_d is the effective voltage across the cell [14], [30], [42], [46]. To overcome C2C variability, iterative write-and-verify process with variable number of steps are used for precise multilevel write operations [45] by subdividing a single long write pulse into a series of short write pulses that each pulse incurs small absolute variation of resistance change. The verify pulses are used to determine the termination of the write process and make the write operation final resistance tolerant to C2C variability. However, to cover the worst-case tail latency caused by C2C variability, much higher latency value should be set for the memory controller. Conventional schemes [45], [46] using incremental voltage pulse ramps guarantee the reachability of the target state but may frequently overshoot much from the target state. Also, these schemes do not fully utilize the feedback information obtained from the verify pulses. The large number of write-and-verify iterations makes the verify pulses take a lot of time [39], [45], [46], enlarging the latency of a multilevel write operation.

To reduce the average number of write-and-verify iterations while tolerating C2C variability during multilevel write operations, we propose a proportional-control variability-adaptive multilevel state tuning (POST) algorithm at the array level. POST adjusts the pulse amplitude in a voltage pulse ramp to tune the selected cell into the target state with fast convergence by leveraging the pulse amplitude-dependent feature of variability, as illustrated in Fig. 10. The key idea is to apply large write pulse when the current state resistance is far away from the target state resistance whereas to apply small write pulse when the current state resistance is close to the target state resistance. This is because if the current state resistance is far away from the target state resistance, the memory cell is tolerable to large resistance variation, and we can apply large pulses but with large absolute variation to make the current resistance go faster to the target resistance range. However, if the current state resistance reaches close to the target state resistance range, the memory cell is vulnerable to variability, and we use small write pulses with small absolute resistance variation to refine the resistance change.

At the array level, since the RESET latency is slightly longer than the SET latency [16], we take the RESET operation as an example to illustrate the detailed design of the POST algorithm. We fix select-line voltage amplitude while varying bit-line voltage pulse amplitude during a multilevel write operation. We further formulate the pulse amplitude V_{RESET} in a voltage pulse ramp applied on the selected bit-lines as

$$V_{\mathrm{RESET}}\left(I^d_{\mathrm{verify}}\right) = k_{\mathrm{RESET}} \cdot \left(I^d_{\mathrm{verify}} - I^d\left(S_{\mathrm{target}}\right)\right) + b_{\mathrm{RESET}}$$

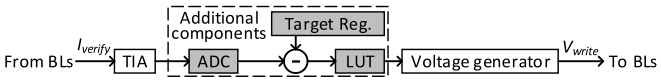

Fig. 11. Illustration of the POST algorithm implementation.

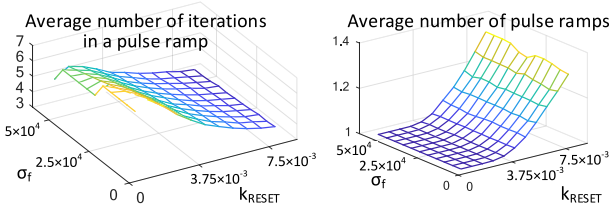

Fig. 12. Tradeoff between the (a) average number of iterations in a voltage pulse ramp and (b) average number of required pulse ramps. σ_f is the variation factor, and k_{RESET} is the proportional coefficient.

where k_{RESET} is the proportional coefficient, I^d_{verify} is the 4-bit digitalized value of the readout current measured from the 4-bit ADC by the verify pulse, $I^d(S_{\text{target}})$ is the 4-bit digitalized value of the readout current at the target state prestored in the target register, and b_{RESET} is the voltage pulse amplitude limitation that guarantees the target state can be timely reached. The value of b_{RESET} is the array basic RESET bias voltage in our configuration (2.55 V). For 1/2 bias scheme, unselected bit-lines and unselected word-lines are biased with $V_{\text{RESET}}(I^d_{\text{verify}})/2$ at the same time. To implement POST, an additional customized 4-bit ADC [47] instead of the original 2-bit ADC for MLC reading is connected to the output terminal of the transimpedance amplifier (TIA) [21], [46] at the end of each selected bit-line, which is to quantize and verify the readout current corresponding to the current cell resistance. Then, the digital value is subtracted with the digital readout value of the target state that is prestored in the target register by a 4-bit subtracter, as shown in Fig. 11. The result is input to a 16-entry lookup table to determine the V_{RESET} value, where the format of each entry is 2-bit integer part with 6-bit decimal part. The V_{RESET} value is taken as the input of the voltage pulse generator [48] for the next write-and-verify iteration. The schematic of POST implementation is shown in Fig. 11. The additional components are globally shared among subbanks [2] in a memory bank. The latency of the V_{RESET} lookup and the write pulse generation [48] is estimated to be less than 2 ns. In a write-and-verify iteration, the write pulse width is fixed as 10 ns, and the verify pulse width is 6 ns, to cover the latency of peripheral circuitry. During SET operations, the bias voltage of the selected select-line can control the gate voltage of the VPAT, limit the SET current through the selected cell, and settle the over-SET problem. Since the gate of VPAT is connected to the select-line, for both RESET and SET operations, we use gate-first scheme, i.e., biasing the select-lines 1-ns before biasing the word-lines and bit-lines, and floating the select-lines 1-ns after floating the word-lines and bit-lines [16].

Proportional coefficient k_{RESET} influences the resistance change in a write-and-verify iteration step and the state overshoot rate in a voltage pulse ramp. If $k_{\text{RESET}} = 0$, it corresponds to the conventional equal-amplitude pulse write scheme. The variation factor σ_f that describes the pulse amplitude-dependent C2C variability of multilevel cells is chosen based on 10-ns write pulse width [44]. As shown in Fig. 12, as k_{RESET} increases, the average number of iterations decreases, but the average number of required pulse ramps increases. Therefore, the value of k_{RESET} shows a tradeoff between the average number of iterations in a voltage pulse ramp and the average number of required pulse ramps. As the overall write latency is proportional to the multiplication of these two metrics, we further use our model to statistically estimate the minimum number of required write-and-verify iterations for adjacent state transitions. The minimum number is achieved when $k_{\text{RESET}} = 7.5 \times 10^{-3}$, and the results are shown in Table II.

TABLE II
MINIMUM AVERAGE NUMBER OF WRITE-AND-VERIFY ITERATIONS, LATENCY, AND ENERGY CONSUMPTION OF ADJACENT STATE TRANSITIONS USING POST (NUMBERS BEFORE BRACKETS) AND RISING PULSE AMPLITUDE STATE TUNING (NUMBERS IN BRACKETS) [45] AT THE ARRAY LEVEL

State transit	3 to 2	2 to 1	1 to 0
Iterations	3.2 (4.5)	2.8 (3.7)	4.4 (6.7)
Latency (ns)	51.2 (72)	44.8 (59.2)	70.4 (107.2)
Energy (nJ)	0.246 (0.43)	0.38 (0.61)	0.55 (1.18)

E. Multilevel Cell Parallel Writing

Finally, we provide a device-architecture level optimization to improve the cell-level write parallelism of multilevel cell resistive cross-point memory arrays. Parallel write operations on a cross-point array are achieved by selecting multiple bit-lines at a time. SET operations and RESET operations have to be performed separately on the same word-line in a cross-point array [7]. For multilevel cell cross-point arrays, the challenge of parallelizing the write operations is that a group of cells starts from and stops with different resistance states. Based on the observation that intermediate resistance states are frequently passed through, we propose an array-level MPW method for resistive cross-point memory arrays, as shown in Algorithm 1. The key idea of MPW is to extract the common write-and-verify iterations among the to-be-written multilevel cells to improve cell-level write parallelism. Once the write process of a selected cell is terminated which is detected by the verify pulse, the corresponding bit-line is biased at the half of the array write bias voltage to mask the cell. To synchronize between cells, the overall write latency is set as the maximum latency among the selected cells. For vertical 3-D cross-point arrays, parallel write operations are performed on the selected plane electrode in our configuration.

The multilevel write latencies of multilevel cells are much more sensitive to the cell effective voltage than those of single-level cells. If we select too much neighboring multilevel cells to write in parallel in an array, the nonuniformity of effective write voltage between these selected cells is significant. In this scenario, the write processes of these selected cells are not identical in a write operation and hard to synchronize. To reduce the nonuniformity of effective write voltage among the

Algorithm 1: Multilevel Cell Parallel Writing in a Cross-Point Memory Array

Input: Final state vector of the cell group with n_w cells: $\overrightarrow{s_f}$
Readout current state vector of the cell group: $\overrightarrow{s_c}$;
Assign total state changes $\overrightarrow{d_{RESET}}$ and $\overrightarrow{d_{SET}}$, where
$d_{RESET}(i) \coloneqq s_f(i) < s_c(i)\ ?\ (s_c(i) - s_f(i)) : 0$ and
$d_{SET}(i) \coloneqq s_f(i) > s_c(i)\ ?\ (s_f(i) - s_c(i)) : 0$, $i \in [1, n_w]$;
while $\overrightarrow{d_{RESET}} \neq \overrightarrow{0}$ **do**
  Common state change $\delta \coloneqq \min\{d_{RESET}(i)\}$, $i \in [1, n_w]$;
  Parallel RESET the cells with $d_{RESET}(i) \neq 0$ using POST, where
  $I^d_{verify} - I^d(S_{target}) \coloneqq$
  $\min\{I^d_{verify}(i) - I^d(s_f(i) + d_{RESET}(i) - \delta)\}$, $i \in [1, n_w]$. Time cost of this step: $t = \max\{t_{cell}(i)\}$, $i \in [1, n_w]$;
  $\overrightarrow{d_{RESET}} \coloneqq \overrightarrow{d_{RESET}} - \overrightarrow{\Delta}$, where $\Delta(i) = \delta$ if $d_{RESET}(i) \neq 0$ and $\Delta(i) = 0$ if $d_{RESET}(i) = 0$;
end
The SET operation process is similar to the above RESET process and is not shown here.

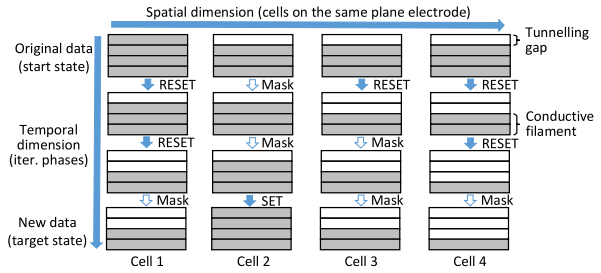

Fig. 13. Spatiotemporal diagram of the MPW process.

selected multilevel cells in a multilevel write operation and precisely control the state of each selected multilevel cell, we choose a relatively smaller number of neighboring multilevel cells to write in parallel in an array (4 in our configuration) than that for single-level cell parallel writing. A detailed illustration of the change process of cell resistance state of a cell group is shown in Fig. 13. Each write-and-verify iteration phase is synchronized. In this example, the parallelism of these phases are 3, 2, and 1, respectively. Sequential multilevel write scheme requires six iteration phases, whereas MPW only needs three phases, thanks to the improved cell-level write parallelism.

V. System-Level Evaluation

A. Setup

We use gem5 simulator [49] integrated with NVMain [50] to evaluate the HD-RRAM design. Table III shows the configuration of the system processor and memory. The physical address-bit format in byte granularity is shown in Fig. 14. We configure the storage-class resistive memory as a DDR-compatible manner. For vertical 3-D cross-point resistive memory, the precharge latency (t_{RP}) is modified as the worst-case charging time of the parasitic capacitance of word-line with plane electrode and bit-line with pillar electrode, to keep steady potential of the interconnects at the beginning of a voltage bias write or read operation [2], [51]. We run gem5 with the SPEC CPU2006 benchmarks for 500 million instructions to evaluate our four optimization methods: 1) DOTA architecture with MAB; 2) VASP; 3) proportional-control state tuning (POST); and 4) MPW. The RRAM

TABLE III
Evaluated System Configuration

Processor core	3 GHz, 4 cores, x86, out-of-order
Level-1 I&D cache	16 KB per core, 2 ways, 2-cycle access, private
Level-2 cache	4 MB, 64-byte block size, 16 ways, 20-cycle access, shared
Memory controller	Open-page policy, FR-FCFS scheduler
Memory organization	Stand-alone, 4 GB, 4 channels, 1 rank per channel, 8 banks per rank, global row buffer size: 64 Bytes
Resistive memory interface & bank timing parameters	DDR3-1066 with zero activate latency and zero restoration latency for memory arrays. The variable write latency (t_{WR}) is set according to the state transition in Table II. Bank read latency: 20 ns.

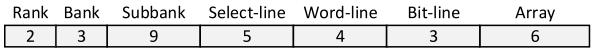

Fig. 14. Address-bit format of the 32-bit address.

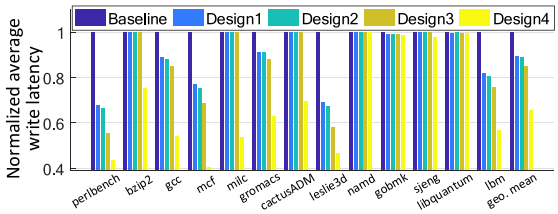

Fig. 15. Average write latency of different schemes normalized to the baseline.

baseline is composed of the state-of-the-art approaches: SITA architecture with MWD [17], $\log_{10}(R)$ equal-difference state partition (ESP) [15], and increasing pulse-amplitude state tuning (IPST) [45]. We implement the basic schemes in the simulator as follows.

1) *Baseline:* SITA-based MWD + ESP + IPST.
2) *Design 1:* DOTA-based MAB + ESP + IPST.
3) *Design 2:* DOTA-based MAB + VASP + IPST.
4) *Design 3:* DOTA-based MAB + VASP + POST.
5) *Design 4:* DOTA-based MAB + VASP + POST + MPW.

B. Performance

Fig. 15 shows the results of average write latency. Generally, the benchmarks that have larger writes-per-kilo-instructions (WPKI) have more significant write latency reduction, e.g., perlbench, mcf, leslie3d, and lbm. DOTA-based MAB (Design 1) and MPW (Design 4) have the most contribution to write latency reduction, because of the significant write velocity improvement and higher cell-level parallelism, respectively. The MPW improvement varies with the average write parallelism of the benchmarks. POST (Design 3) also has a remarkable contribution to write latency reduction, benefiting from the reduction of write-and-verify iterations compared with IPST. Compared with the baseline RRAM, HD-RRAM reduces the average write latency by 34.1% across the benchmarks.

As write operations are accelerated, the read latency also slightly reduced by 5%, since the request queuing latency is reduced. The normalized average memory access latency is only a little higher than the normalized average write latency, as shown in Fig. 16. This is because the multilevel write

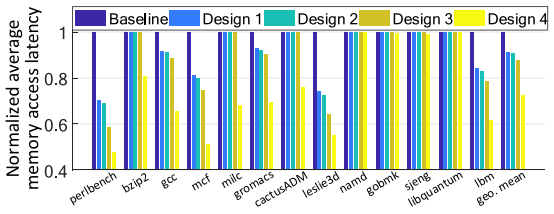

Fig. 16. Memory access latency of different schemes normalized to baseline.

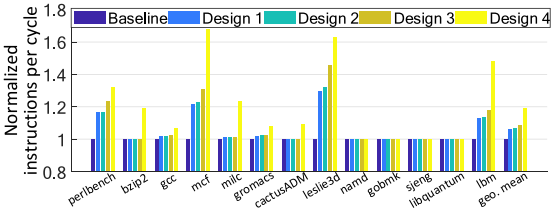

Fig. 17. Instructions per cycle of different schemes normalized to the baseline.

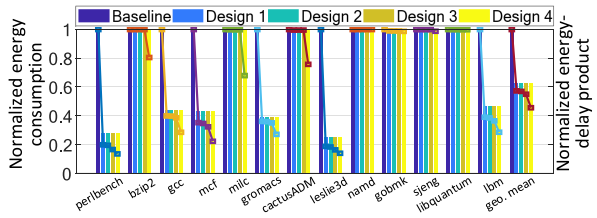

Fig. 18. Average energy consumption per memory access (bar plot) and EDP (line plot) of different schemes normalized to baseline.

latency is much longer than the multilevel read latency and the write latency dominates the memory access latency. HD-RRAM reduces the average memory access latency by 27.5% on average across the benchmarks.

The instructions per cycle (IPC) result is shown in Fig. 17. The IPC improvement relates to the write latency reduction and also the intensity of write access. Some benchmarks have significant reduction of memory access latency but do not have significant IPC improvement, due to small portion of memory write access, e.g., gcc and gromacs. The average IPC improvement of HD-RRAM system is 19.4% across the benchmarks, compared with the baseline.

C. Energy Consumption

The results of the energy consumption and energy-delay product (EDP) of the HD-RRAM system are shown in Fig. 18. Here, EDP is used to reveal the energy efficiency of memory access operations. The energy consumption is mainly reduced by the DOTA-based MAB (Design 1), thanks to the reduction of array bias voltage and the distributed voltage delivery. Compared with the baseline, the energy reduction and EDP reduction of the HD-RRAM system are 37.2% and 54.4% on average across the benchmarks, respectively.

D. Memory Density

The memory density of HD-RRAM can achieve 3.68 Gb·mm^{-2} at 45-nm feature size, and the density will further improve as the feature size scaling down. Moreover, compared with the designs that only adopt one or two high-density approaches, such as multilevel cell 2-D one-transistor–one-resistor (1T1R) resistive memory [46], single-level cell 2-D cross-point resistive memory [6], and single-level cell 3-D cross-point resistive memory [17] at the 45-nm feature size, HD-RRAM improves the memory density by 24×, 32×, and 2×, respectively.

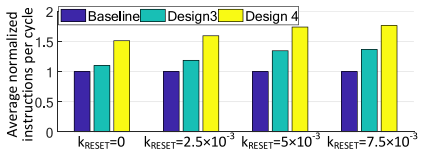

Fig. 19. Performance sensitivity to the proportional coefficient in POST over four write intensive benchmarks (perlbench, mcf, leslie3d, and lbm).

TABLE IV
EXTRA AREA/POWER/LATENCY OVERHEAD OF THE BANK-LEVEL PERIPHERAL CIRCUITRY OF HD-RRAM SYSTEM

	DOTA-based MAB	VASP	POST	MPW
Area (%)	-6.5	+0.059	+3.9	+1.4
Power (mW)	-147.2	+0.001	+70.2	+12.2
Latency (ns)	0.0	+0.1	+5.63	+0.20

E. Sensitivity Analysis

The proportional coefficient k_{RESET} in POST tradesoff between the number of pulses in a voltage ramp and the number of required voltage ramps. As we boost the array bias voltage at the beginning of a RESET process by enlarging k_{RESET}, the switching velocity improves but the variability also increases. So there is a latency tradeoff between the average number of write-and-verify iterations in a voltage pulse ramp and the average number of required pulse ramps. Fig. 19 shows the sensitivity of performance improvement to different k_{RESET} values in the POST scheme from 0 to 7.5×10^{-3}. Boosting k_{RESET} in POST achieves fast convergence to the target state without significantly increasing the state overshoot rate. The performance sensitivity analyses on other parameters (e.g., the array size and the number of cells to write in parallel) are similar to those in prior works [6], [15].

F. Hardware Implementation Cost

We implement the hardware components of the HD-RRAM system in Synopsys Design Compiler by Verilog HDL to evaluate the extra hardware cost compared with the baseline, with respect to the area, power consumption, and latency at bank level. The memory array peripheral circuitry is evaluated based on TSMC 130-nm cell library and scaled to 22-nm technology size. The results are summarized in Table IV. First, to implement DOTA-based MAB, the extra components for each memory array include a top-layer VPAT array, a top-layer select-line decoder to control the top-layer VPAT array, and a top-layer bit-line multiplexer. These components are the same as the bottom part underneath the memory array, and the top and the bottom components are working in parallel. Thus, the top peripheral components do not incur extra area and latency cost. The extra peripheral circuitry can be hidden underneath the memory arrays by sharing ADCs among sub-banks. Moreover, benefiting from the current-dividing effects

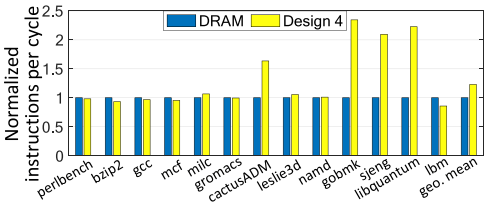

Fig. 20. Instructions per cycle for HD-RRAM system across different benchmarks normalized to the DDR3 DRAM system.

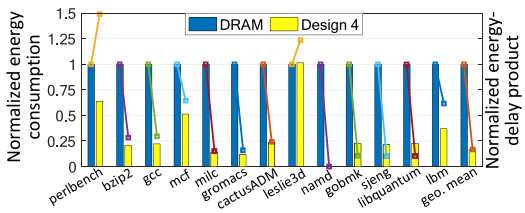

Fig. 21. Average energy consumption per memory access (bar plot) and EDP (line plot) of the HD-RRAM system across different benchmarks normalized to the DDR3 DRAM system.

and distributed voltage delivery, the size of each voltage driver which is proportional to the line current [6], [12], [22] is even reduced by 48.3%. Owing to that, the total area of peripheral circuitry is reduced by 6.5%, and the power consumption of the bank-level peripheral circuitry is reduced by 147.2 mW. Second, to implement VASP, we only need to shift the reference input of the read reference comparators [6], [21] that are connected to the TIAs at the end of the selected bit-lines. The readout current values of the two intermediate states are input to the reference comparator [6], [15] to determine the termination of the write-and-verify iteration process when the verify pulse is applied. Therefore, for each memory array, VASP only requires a 2-entry 32-bit lookup table for recording the readout current values in unit of nA of the two intermediate resistance states. Third, additional components to implement POST for writing a cache-line in a 1-GB bank include 256 4-bit ADCs, 256 4-bit target registers, 256 4-bit subtractors, and 64 16-entry 8-bit lookup tables. A customized 4-bit ADC [47] in a bank consumes extra 0.0137% chip area, 0.254-mW power, and 4-ns latency. In total, the peripheral circuitry including the ADCs to implement POST in a bank takes extra 3.9% chip area, 70.2-mW power, and 5.63-ns latency. Finally, the peripheral logic to support MPW in a bank consumes extra 1.4% chip area, 12.2-mW power, and 0.2-ns latency. These extra hardware costs are considered in the system-level evaluation.

G. Comparison With DRAM

1) DDR3 DRAM: We add the simulation of DDR3 DRAM in the NVMain to compare with HD-RRAM. The normalized IPC result is shown in Fig. 20. For most of the benchmarks, the IPC for HD-RRAM is comparable to that for DRAM. For some read-intensive benchmarks, the IPC for HD-RRAM is even higher than that for DRAM. Overall, the IPC for HD-RRAM system is 1.23 times of that for the DDR3 DRAM system on average across different benchmarks. Besides, the normalized energy consumption and EDP results are shown in Fig. 21. Generally, HD-RRAM has great energy reduction over DRAM. For some benchmarks, the normalized EDP reduction of RRAM is less than the normalized energy reduction, since RRAM multilevel write latency is longer than DRAM write latency. On average, the EDP of HD-RRAM system is 16.7% of that of the DDR3 DRAM system across different benchmarks. Thus, HD-RRAM system has superior energy efficiency and performance advantage over DDR3 DRAM system.

2) HBM DRAM: We further add the gem5 simulation with 3-D through-silicon via (TSV)-based high-bandwidth memory (HBM) DRAM [52]. Here, the TSV parasitic capacitance of HBM is not considered in the simulation. The evaluation results show that the IPC for HD-RRAM is 52.6% of that for HBM DRAM system on average across the benchmarks. The HBM DRAM is integrated on the processor in our simulation, whereas HD-RRAM is configured as standalone and placed off-chip. HBM utilizes a 2-D interface at die level to improve memory access parallelism and thus enlarges the bandwidth, whereas HD-RRAM does not use the wide interface. The design objective of HD-RRAM is different from that of HBM DRAM. The design objective of HBM DRAM is to improve memory access bandwidth by improving interface parallelism at die level to expand the conventional DDR DRAM and provide parallel memory access for bandwidth-bounded processors, while not aiming at reducing latency. On contrary, the design objective of HD-RRAM is to reduce write latency of high-density resistive memory at the memory array level, which is orthogonal to improve memory access parallelism by extending interface.

3) Write Endurance Concern: The write endurance of RRAM devices is up to 10^{10} write cycles [6], [13], which is lower than that of the storing-charge-based DRAM capacitors that can endure around 10^{16} writes [12]. This suggests that RRAM should be mainly applied in storage-class memory systems [2]. But the limited write endurance problem of RRAM might become a reliability challenge when RRAM is used for main memory. Table-based wear-leveling scheme can be used to improve the lifetime of cross-point memory arrays by exploiting the nonuniformity of write wear-out as a function of cell location [53]. Our proposed scheme aims to reduce the write latency of high-density resistive memory arrays at the physical-device level and is orthogonal to the system-level wear-leveling schemes.

VI. Related Work and Discussion

Multilevel resistive memory cells improve memory density by subdividing intermediate resistance states from the two boundary states. Xu *et al.* [15] proposed the ESP scheme for multilevel cells. Alibart *et al.* [45] proposed an IPST scheme for the iterative write-and-verify process of a standalone multilevel cell. Hu *et al.* [46] increased the word-line pulse voltage and bit-line pulse voltage to realize multilevel states during SET operations in 1T1R memory arrays. Yao *et al.* [32] achieved precise multilevel write operations on eight 1T1R memory arrays. Zhang *et al.* [54] proposed to lower the gate voltage and enlarge the width/length ratio of the access transistors in the single-level cell 1T1R memory array to reduce the variability during SET operations.

Access-transistor-free cross-point memory arrays can achieve higher memory density than 1T1R memory arrays. 2-D cross-point memory arrays with size of 17×17 [55], 20×20 [56], 24×24 [57], 32×32 [58]–[60], 48×48 [61], 54×108 [62], and 64×64 [63] were demonstrated. 1TnR memory array with multilevel cells was also demonstrated [36]. 3-D memory array integration further improves memory areal density by stacking memory layers. 3-D cross-point memory arrays with size of $2 \times 8 \times 8$ [64] and $2 \times 10 \times 10$ [65] were demonstrated. Yu *et al.* [27] compared three types of 3-D cross-point arrays with respect to effective voltage, read margin, and write energy. Deng *et al.* [28] studied design guidelines for vertical 3-D resistive memory. Chen *et al.* [66] profiled the voltage drop distribution on the selected slice of vertical 3-D cross-point arrays. Xu *et al.* [24] built a static model for vertical 3-D cross-point arrays. Xu *et al.* [17] proposed an MWD scheme based on the SITA architecture to reduce the IR drop along the selected plane electrode by connecting four sides of the distributed word-line to the voltage source at a time. Gao *et al.* [34] demonstrated cell-grouping write and read array bias schemes for the single-level cell vertical 3-D cross-point memory array integrated with a single VPAT array at the bottom, where the write bias scheme is derived from unselected word-line 1/2 biasing with unselected bit-line floating scheme, and the read bias scheme is derived from unselected word-line grounding read-in-a-row scheme. Both write and read bias schemes are to the single side of interconnects. Hexagonal pillar layout, center landing of compact staircase contacts, and interarray global-shared-word-line memory array architecture were designed to improve areal density [26], [38], [67], [68]. The hexagonal pillar layout complicates the alignment of select-lines and bit-lines to the pillar electrodes and increases the array modeling complexity and operation simulation time.

Different from the existing work, our proposed memory array architecture features double vertical-pillar-access-transistor arrays, and our distributed array operating bias scheme features multisided and asymmetric voltage sources connecting to different ends or sides of a interconnect line or plane. Besides, our solution is to reduce the latency of write operations on multilevel cell 3-D cross-point memory arrays by decoupling the array-level and cell-level nonideality issues and coping with these nonidealities in each part of the design stages, respectively, by dynamic operation optimization.

VII. Conclusion

From the perspective of the interactions between interconnects and devices in memory arrays, we analyzed the impacts of the interactions between array-level and cell-level nonideal device properties (IR drop, sneak current, and device variability) on the performance and reliability of write operations and the design challenges of memory array operation scheme, when we compose MLC, cross-point memory array structure, and 3-D memory array integration approaches together. We proposed HD-RRAM, a nonideality-tolerant ultrahigh-density resistive memory architecture, to improve the performance and reliability of multilevel write operations by static parameter and dynamic operation co-optimization. Evaluations showed that HD-RRAM significantly reduces both memory access latency and energy consumption on average across the benchmarks compared with the aggressive baseline.

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